C1 Cont.

a second layer of nickel on said alloy layer, said second nickel layer deposited to be suitable for bending of said lead segments, wire bonding, and solder attachment;

a layer of palladium, said palladium layer deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound; and

gold selectively plated on segments of said leadframe intended for solder attachment.

C2

11. (amended) A packaged semiconductor device comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium;

said leadframe further having gold selectively plated on segments of said leadframe intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

14. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

Please add the following new claims:

C3

23. (new) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

C3 cont.

24. (new) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment, wherein said layer of palladium has a thickness in the range of about 0.03% to about 6% of a thickness of said nickel layer;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

25. (new) The packaged semiconductor device, wherein said layer of nickel has a thickness in the range of about 500 nm to about 3000 nm and said palladium layer has a thickness in the range of about 10 nm to about 30 nm.

D1

26. (new) The packaged semiconductor device, wherein said gold has a thickness in the range of about 6% to about 50% of said thickness of said palladium layer.

REMARKS

Claims 1-13 and 15 were pending in this Application. Claims 1, 2 and 11 have been amended. Claims 14 and 16-22 have been cancelled. Claims 23-26 have been added for this Continuing Patent Application. Applicant respectfully requests entry and consideration of these claims.

The following remarks are in response to the Office Action mailed 6/28/2002 and are offered as a full and complete response to that action.